Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 7-8, 16 and 19 have been amended. Claims 4, 6 and 20-24 have been cancelled. No claims have been added. Therefore, claims 1-3, 5 and 7-19 are presented for examination.

Specification

The title has been amended to appear in better condition for allowance. The objection to the title has been sustained since the first Office Action for present application. Applicants submit that the presently amended title is clearly indicative of the invention to which the claims are directed. Applicants respectfully request that the objection to the title be withdrawn.

35 U.S.C. §112 Rejection

Claim 7 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Claim 7 has been amended to appear in better form for allowance. Applicants respectfully request that the §112 rejection be withdrawn for claim 7.

35 U.S.C. §103(a) Rejection

Claims 1-3, 5-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thomas et al., U.S. Patent No. 5,752,011 ("Thomas") in view of Shiell et al., U.S. Patent No. 6,138,232 ("Shiell"). Applicants submit that the present claims are patentable over Thomas in view of Shiell.

Thomas discloses a method for controlling a processor's clock frequency so as to prevent overheating. The invention attempts to maximizes the processing speed of the processor while preventing overheating. In a preferred embodiment, the invention monitors a processor's activity and its temperature. When there is no activity for the processor, a slowed clock frequency is used, thereby saving power and lowering the thermal heat produced by the processor. When there is activity for the processor, a fast clock frequency is used. However, when prolonged activity (i.e., sustained fast clock frequency) causes the processor's temperature to become dangerously high for proper operation, the clock frequency is reduced so as to maintain processing speed at a reduced speed while preventing overheating. See Thomas at Abstract.

Shiell discloses a method of operating a microprocessor. The microprocessor accepts an interrupt from one of a plurality of interrupt sources. The microprocessor then operates at a rate dependent upon the interrupt source. The rate of power consumption by the microprocessor corresponds to the selected rate of instruction operation. A rate table stores a table of interrupt source to rate of instruction operation. The rate table is accessed upon receipt of an interrupt to obtain a rate of instruction operation corresponding to the interrupt source. The microprocessor is then operated at the recalled rate. The rate table may be a read only memory or a read/write memory loaded upon initiation of the microprocessor. The rate of instruction operation may be controlled by a rate of instruction dispatch. For a superscalar microprocessor capable of concurrently executing plural instructions simultaneously the rate of instruction operation may be set by setting a number of instructions dispatched per instruction cycle. This could include dispatching instructions to a number of execution units based upon the selected rate. Electric power consumption is

conserved by powering only those execution units to which instructions are dispatched. See Shiell at col. 1, ll. 45 – col. 2, ll. 25.

Claim 1 recites:

> A system comprising:
> a central processing unit (CPU) including power management logic to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold; and
> programmable array logic (PAL) to operate as an interrupt handler to control the CPU upon receiving an interrupt.

Applicants submit that Thomas does not disclose or suggest a CPU to execute a first quantity of instructions per cycle whenever a temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold, as recited by claim 1. Thomas discloses a method for controlling a processor's clock frequency in order to prevent overheating. In contrast, claim 1 recites that a CPU executes a first quantity of instructions per cycle whenever a temperature of the CPU exceeds a predetermined threshold and executes a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold. There is no correlation between clock frequency and instructions executed per cycle. In fact, the number of instructions per cycle could stay the same even though the clock frequency has changed. Therefore, changing the clock frequency in order to control temperature is not equivalent to changing the quantity of instructions executed by the CPU in response to a change in temperature.

Furthermore, Shiell does not disclose or suggest a CPU to execute a first quantity of instructions per cycle whenever a temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold. Shiell discloses operating in a partial or full execution mode in response to changes in power consumption by a processor. Thomas discloses changing a processor's clock frequency (not the quantity of instructions executed per cycle) in response to changes in the processor's temperature. Therefore, there would have been no motivation to use the features of Shiell in Thomas because they apply to different applications.

In addition, Shiell discloses changing instructions per cycle in response to changes in power consumption, which is not the same as changing instructions per cycle in response to changes in temperature.

Neither Thomas nor Shiell disclose or suggest the cited feature of claim 1. Therefore, applicants submit that Thomas and Shiell, individually or in combination, do not disclose or suggest a CPU to execute a first quantity of instructions per cycle whenever a temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold, as recited in claim 1. Therefore, claim 1 is patentable over Thomas in view of Shiell.

Claims 2-3, 5 and 7 depend from claim 1 and include additional limitations. Therefore, claims 2-3, 5 and 7 are also patentable over Thomas in view of Shiell.

Claims 8 and 16, include features similar to those recited in claim 1, namely, the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle

whenever the temperature of the CPU is below the predetermined threshold. Therefore, applicants submit that claims 8 and 16 are patentable over Thomas in view of Shiell, for the reasons stated above with respect to claim 1. Claims 9-15 and 17-19 depend from claims 8 and 16, respectively. As a result, claims 9-15 and 17-19 are also patentable over Thomas in view of Shiell.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: August 31, 2005

Ashley R. Ott
Reg. No. 55,515

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980